MONARCH: Next Generation SoC (Supercomputer on a Chip)

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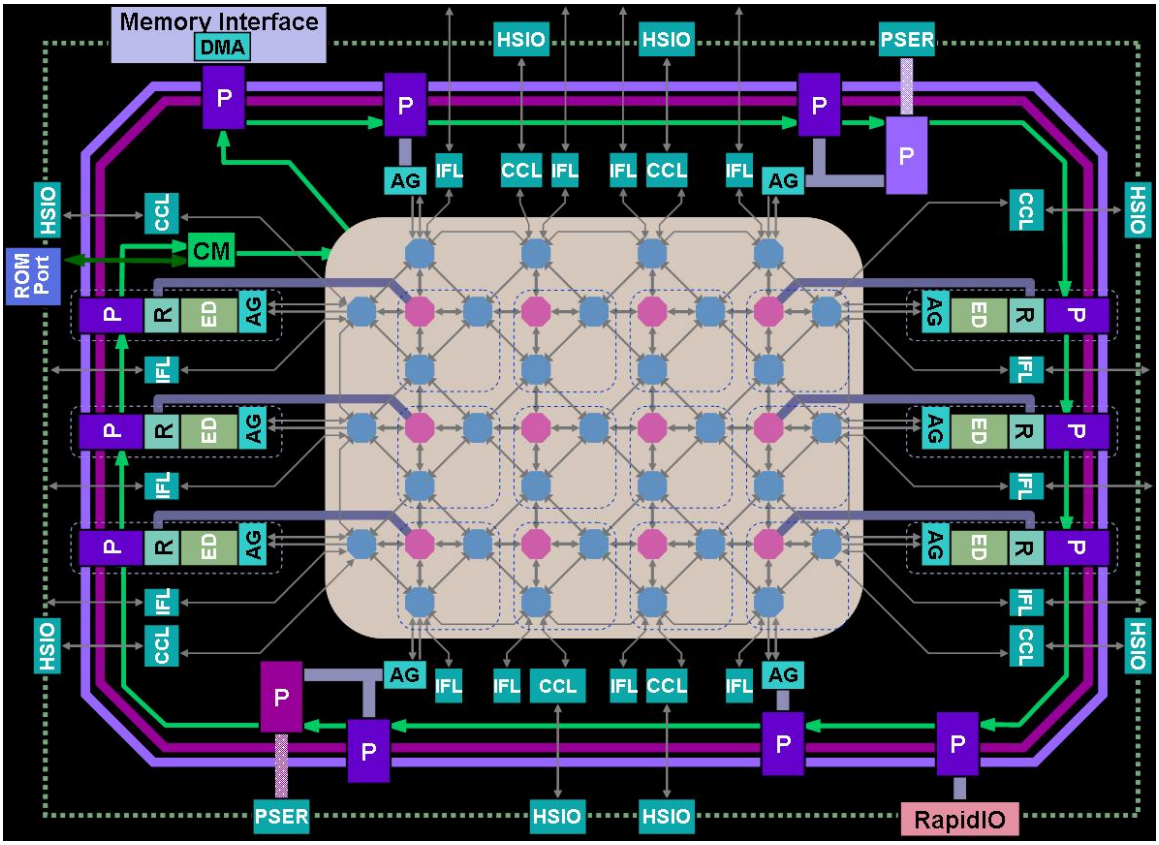
The MONARCH project is sponsored by DARPA under the Polymorphous Computer Architecture Program. MONARCH is developing a revolutionary chip distinguished from other PCA systems by unifying two radically different architectures into a single flexible VLSI device. MONARCH architecture combines the DIVA PIM architecture, developed by USC/ISI as part of the DARPA-sponsored Data Intensive Program, and HPPS (High Performance Processing System) developed by Raytheon with IRAD funds.

We previously presented the motivation for merging these two architectures (HPEC 2002). We have since developed the detailed specifications for the micro architecture of the MONARCH chip and also the software environment, run time system and on-chip communication network. Furthermore, we have completed the evaluation of several benchmarks and we have shown that the MONARCH architecture is capable of achieving a very high stability factor that allows the MONARCH architecture to process data at near peak throughput speeds.

The current version of the MONARCH architecture has undergone continued refinement and the latest performance estimates based on IBM's Cu 08 (90 nanometer CMOS) technology are included in the figure below:



- 333 MHz Clock
- 192 ops/clock
- 64 GFLOPS
- 64 GOPS
- 12 MBytes DRAM
- 124 KBytes SRAM
- 96 MALU
- 8-50 Watts

Report Documentation Page

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Although these performance estimates are lower than the initial peak performance estimates presented earlier, the energy efficiency (measured in OPS/Watt or FLOPS per Watt) of the VLSI implementation is still much higher than most current and near term commercial microprocessors.

We will present details about the micro architecture, particularly the on-chip and off-chip networks as well as the runtime system, the component-based software development environment and MONARCH's performance on the Lincoln Laboratories PCA kernels and benchmarks as predicted by the MONARCH simulator. We will also present an overview of MONARCH's model for morphing and the morphing capabilities envisioned for the first prototype.

Abstract
Agenda

Reconfigurable Computing
MONARCH/MCHIP
High Efficiency Embeddable TeraFlops Polymorphous Computing Architecture

Mike Vahey / John Granacki

Raytheon / USC-ISI

September 29, 2004

MOrphable Networked micro-ARCHitecture

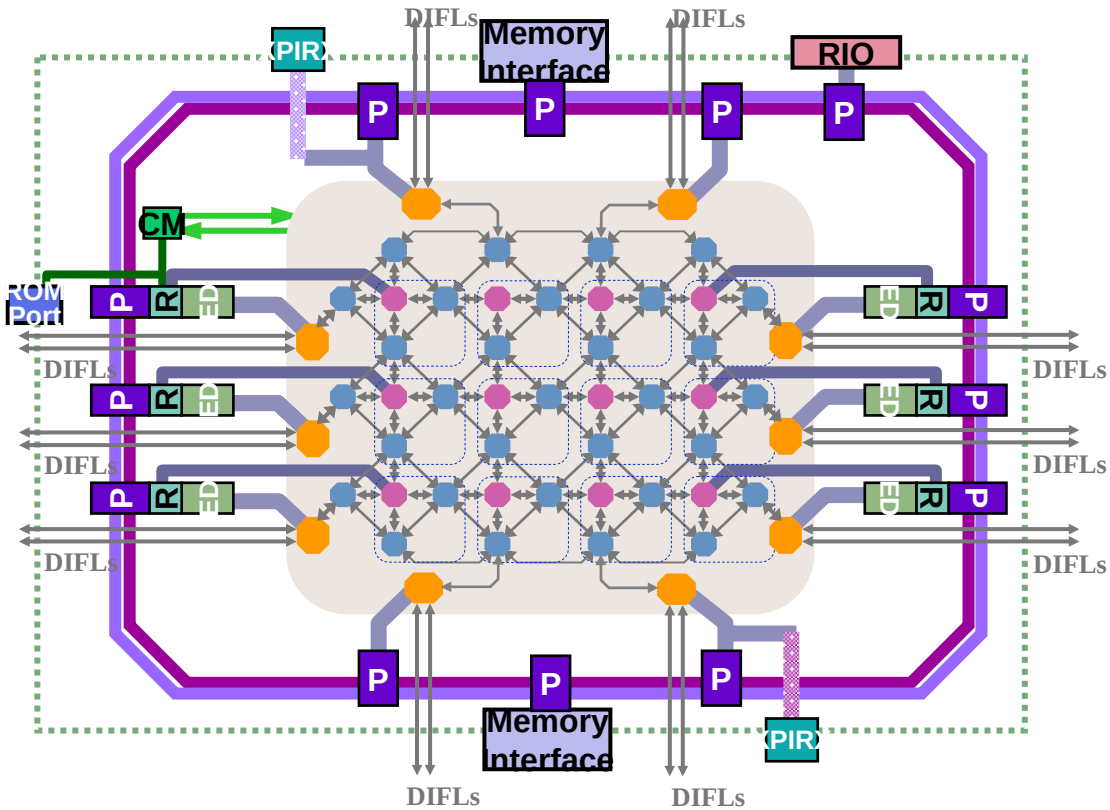
Exogi

MONARCH System on a Chip

RISC, DRAM, Computing Array, Streaming I/O

Raytheon

Space and Airborne Systems



- Alternative to ASICS or custom hardware
- Demonstrated for RADAR, COM, EO
- Late algorithm freeze – retains programmability
- Energy efficiency: 3-6 GFLOPS/W

- Polymorphous Architecture
- Multiple programming modes
  - Reconfigurable, streaming DF
  - RISC scalar
  - RISC SIMD (Altivec like)
- 6 RISC processors
- Reconfigurable Computing
  - 96 adders fixed and float
  - 96 multipliers
  - 124 dual port memories
  - 248 address generators
- 12 MBytes on chip DRAM
- 14 DMA engines
- RapidIO interface
- 20 DIFL ports (1.3 GB/s ea)
- Power 8-50 W (nominal)
- Throughput 64 GFLOPS peak

ISI Information Sciences Institute

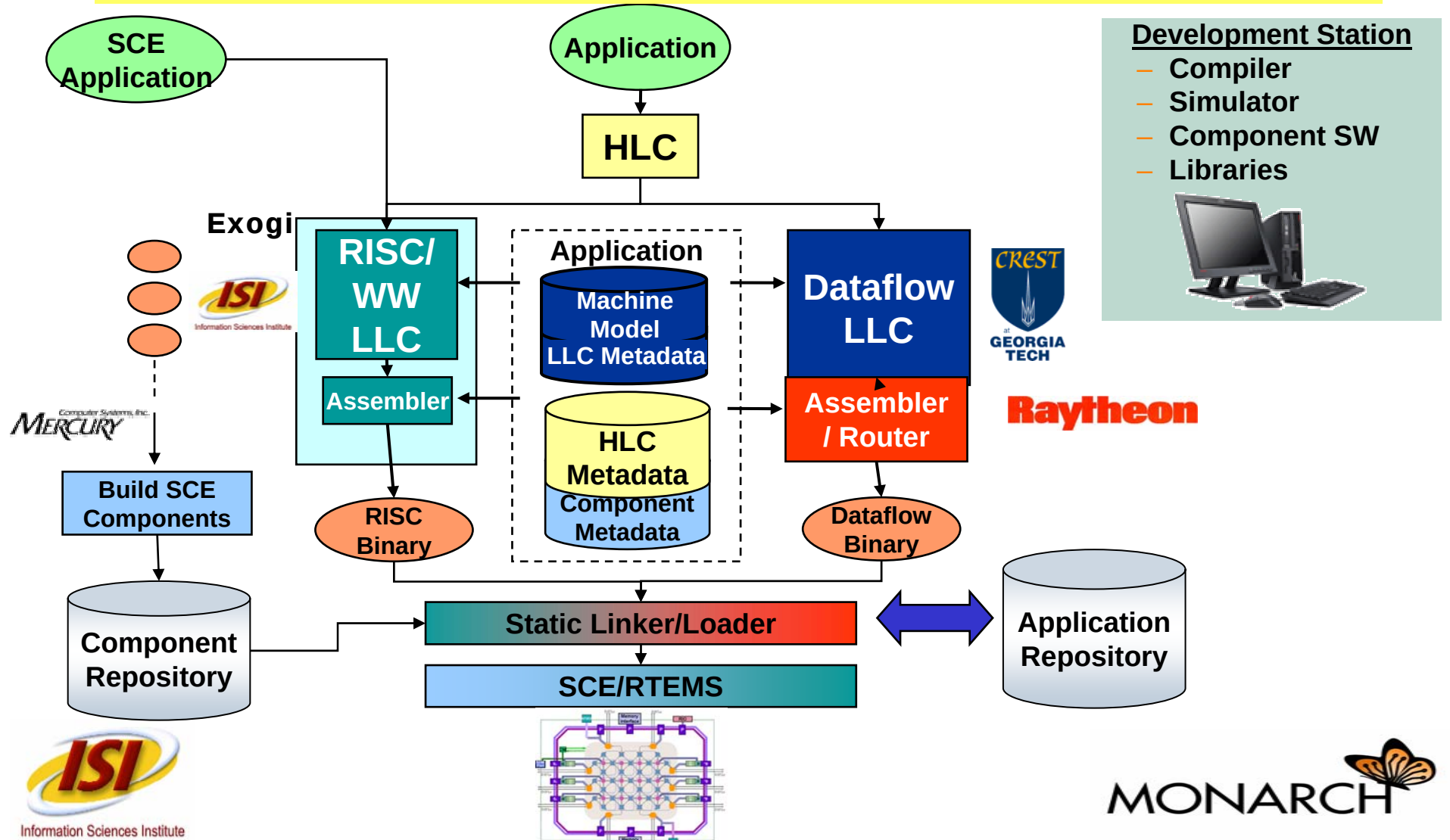
MONARCH

Application Development Environment & Workstation

DARPA

Raytheon
Space and Airborne Systems

Multiple Computing Modes adapt to application needs:
1) RISC Scalar, 2) Wide Word, 3) Reconfigurable Data Flow

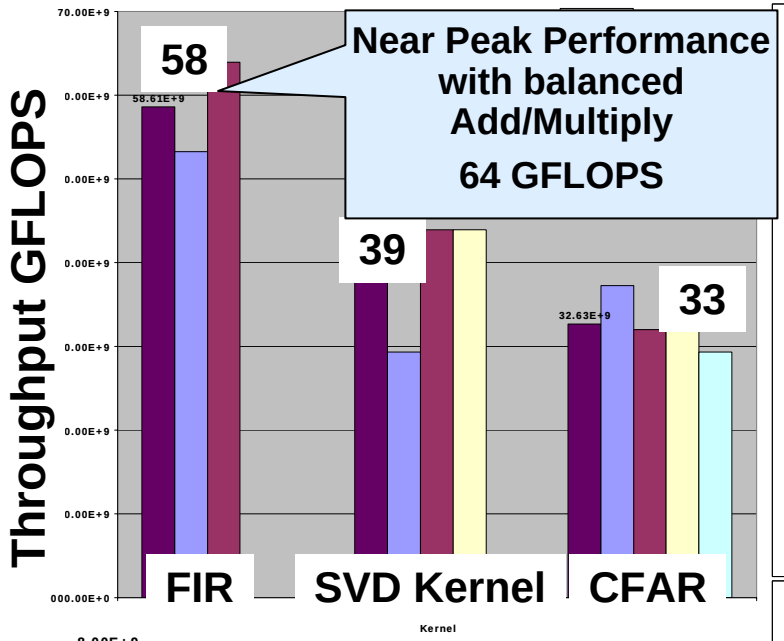


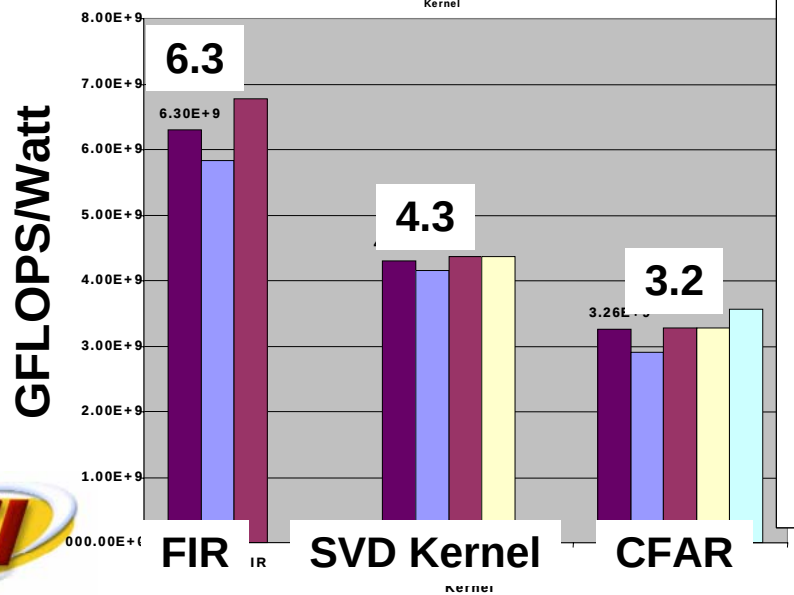
MONARCH Performance on Lincoln Lab Benchmark Suite

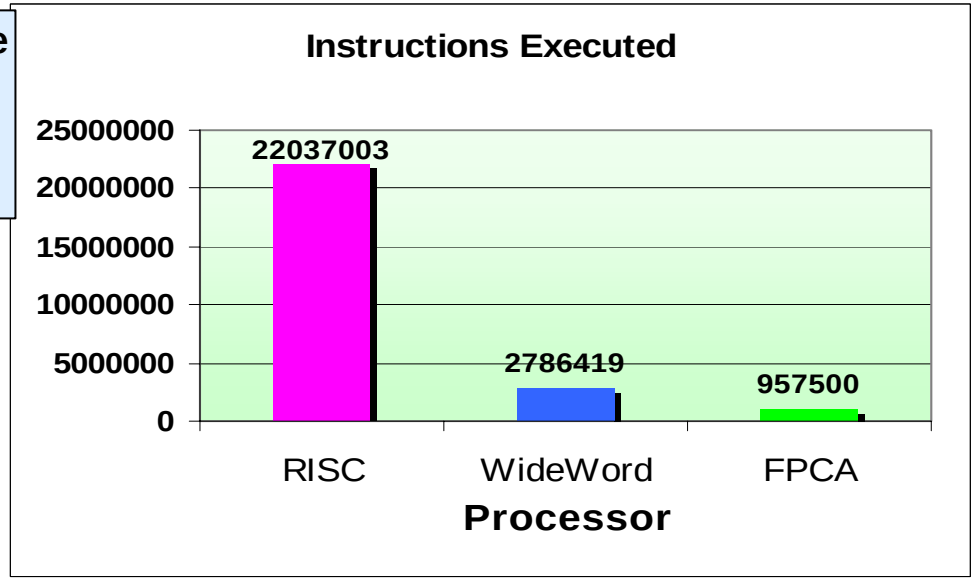
DARPA

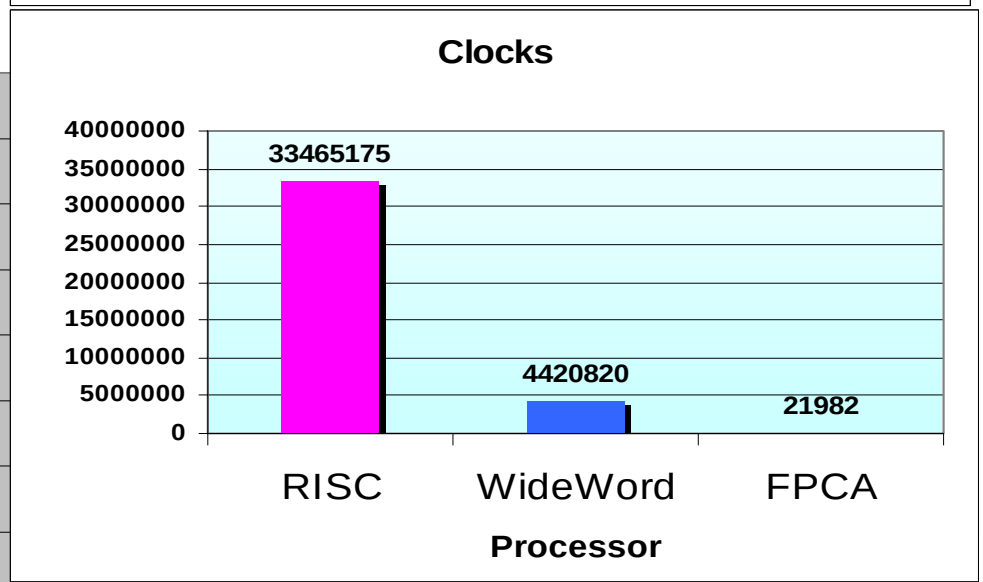
Raytheon

Space and Airborne Systems









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